

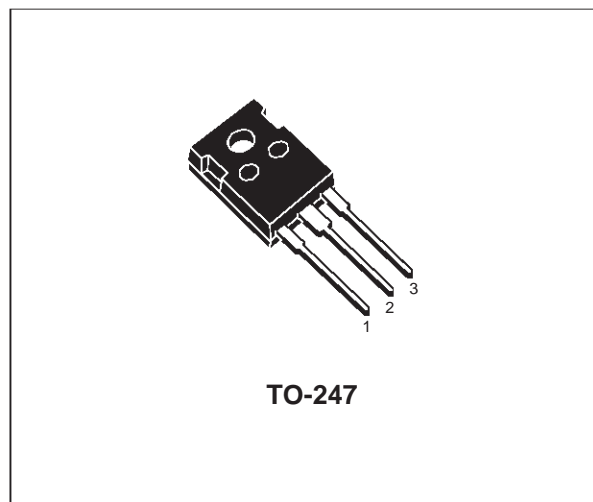
## N - CHANNEL ENHANCEMENT MODE POWER MOS TRANSISTOR

TYPE	V <sub>DSS</sub>	R <sub>DS(on)</sub>	I <sub>D</sub>
STW50N10	100 V	< 0.035 Ω	50 A

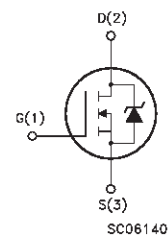
- TYPICAL R<sub>DS(on)</sub> = 0.027 Ω
- AVALANCHE RUGGED TECHNOLOGY
- 100% AVALANCHE TESTED
- REPETITIVE AVALANCHE DATA AT 100°C
- HIGH CURRENT CAPABILITY
- 175°C OPERATING TEMPERATURE
- APPLICATION ORIENTED CHARACTERIZATION

### APPLICATIONS

- HIGH CURRENT, HIGH SPEED SWITCHING
- POWER MOTOR CONTROL
- DC-DC & DC-AC CONVERTERS
- SYNCHRONOUS RECTIFICATION



### INTERNAL SCHEMATIC DIAGRAM



### ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V <sub>DS</sub>	Drain-source Voltage (V <sub>GS</sub> = 0)	100	V
V <sub>DGR</sub>	Drain- gate Voltage (R <sub>GS</sub> = 20 kΩ)	100	V
V <sub>GS</sub>	Gate-source Voltage	± 20	V
I <sub>D</sub>	Drain Current (continuous) at T <sub>c</sub> = 25 °C	50	A
I <sub>D</sub>	Drain Current (continuous) at T <sub>c</sub> = 100 °C	35	A
I <sub>DM</sub> (●)	Drain Current (pulsed)	200	A
P <sub>tot</sub>	Total Dissipation at T <sub>c</sub> = 25 °C	180	W
	Derating Factor	1.2	W/°C
T <sub>stg</sub>	Storage Temperature	-65 to 175	°C
T <sub>j</sub>	Max. Operating Junction Temperature	175	°C

(●) Pulse width limited by safe operating area

I<sub>SD</sub> ≤ 60 A, di/dt ≤ 200 A/μs, V<sub>DD</sub> ≤ V<sub>(BR)DSS</sub>, T<sub>j</sub> ≤ T<sub>JMAX</sub>

**STW50N10****THERMAL DATA**

$R_{thj-case}$	Thermal Resistance Junction-case	Max	0.83	$^{\circ}C/W$
$R_{thj-amb}$	Thermal Resistance Junction-ambient	Max	30	$^{\circ}C/W$
$R_{thc-sink}$	Thermal Resistance Case-sink	Typ	0.1	$^{\circ}C/W$
$T_j$	Maximum Lead Temperature For Soldering Purpose		300	$^{\circ}C$

**AVALANCHE CHARACTERISTICS**

Symbol	Parameter	Max Value	Unit
$I_{AR}$	Avalanche Current, Repetitive or Not-Repetitive (pulse width limited by $T_j$ max, $\delta < 1\%$ )	50	A
$E_{AS}$	Single Pulse Avalanche Energy (starting $T_j = 25^{\circ}C$ , $I_D = I_{AR}$ , $V_{DD} = 25 V$ )	400	mJ

**ELECTRICAL CHARACTERISTICS** ( $T_{case} = 25^{\circ}C$  unless otherwise specified)

OFF

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
$V_{(BR)DSS}$	Drain-source Breakdown Voltage	$I_D = 250 \mu A$ $V_{GS} = 0$	100			V
$I_{DSS}$	Zero Gate Voltage Drain Current ( $V_{GS} = 0$ )	$V_{DS} = \text{Max Rating}$ $V_{DS} = \text{Max Rating}$ $T_c = 125^{\circ}C$			1 10	$\mu A$ $\mu A$
$I_{GSS}$	Gate-body Leakage Current ( $V_{DS} = 0$ )	$V_{GS} = \pm 20 V$			$\pm 100$	nA

ON (\*)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
$V_{GS(th)}$	Gate Threshold Voltage	$V_{DS} = V_{GS}$ $I_D = 250 \mu A$	2	3	4	V
$R_{DS(on)}$	Static Drain-source On Resistance	$V_{GS} = 10 V$ $I_D = 25 A$		0.027	0.035	$\Omega$
$I_{D(on)}$	On State Drain Current	$V_{DS} > I_{D(on)} \times R_{DS(on)max}$ $V_{GS} = 10 V$	50			A

**DYNAMIC**

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
$g_{fs} (*)$	Forward Transconductance	$V_{DS} > I_{D(on)} \times R_{DS(on)max}$ $I_D = 25 A$	20	45		S
$C_{iss}$	Input Capacitance	$V_{DS} = 25 V$ $f = 1 MHz$ $V_{GS} = 0$		4100	5200	pF
$C_{oss}$	Output Capacitance			600	800	pF
$C_{rss}$	Reverse Transfer Capacitance			150	200	pF

## ELECTRICAL CHARACTERISTICS (continued)

## SWITCHING ON

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
$t_{d(on)}$	Turn-on Time	$V_{DD} = 50\text{ V}$ $I_D = 25\text{ A}$		25	35	ns
$t_r$	Rise Time	$R_G = 4.7\ \Omega$ $V_{GS} = 10\text{ V}$		75	105	ns
$Q_g$	Total Gate Charge	$V_{DD} = 80\text{ V}$ $I_D = 50\text{ A}$ $V_{GS} = 10\text{ V}$		120	170	nC
$Q_{gs}$	Gate-Source Charge			20		nC
$Q_{gd}$	Gate-Drain Charge			50		nC

## SWITCHING OFF

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
$t_{r(off)}$	Off-voltage Rise Time	$V_{DD} = 80\text{ V}$ $I_D = 50\text{ A}$		30	45	ns
$t_f$	Fall Time	$R_G = 4.7\ \Omega$ $V_{GS} = 10\text{ V}$		35	50	ns
$t_c$	Cross-over Time			65	95	ns

## SOURCE DRAIN DIODE

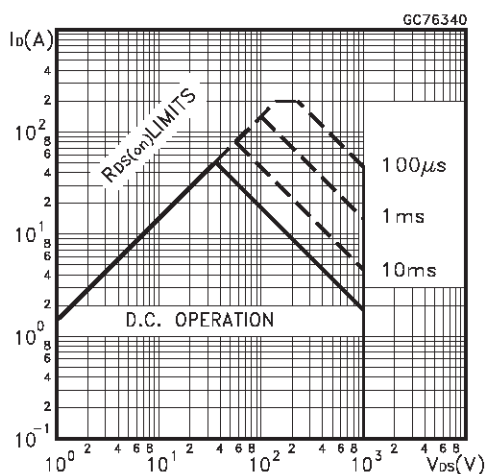
Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
$I_{SD}$	Source-drain Current				50	A
$I_{SDM}(\bullet)$	Source-drain Current (pulsed)				200	A
$V_{SD}(\ast)$	Forward On Voltage	$I_{SD} = 50\text{ A}$ $V_{GS} = 0$			1.5	V
$t_{rr}$	Reverse Recovery Time	$I_{SD} = 50\text{ A}$ $di/dt = 100\text{ A}/\mu\text{s}$ $V_{DD} = 30\text{ V}$ $T_j = 150\text{ }^\circ\text{C}$			200	ns
$Q_{rr}$	Reverse Recovery Charge				1.4	$\mu\text{C}$
$I_{RRM}$	Reverse Recovery Current				14	A

(\*) Pulsed: Pulse duration = 300  $\mu\text{s}$ , duty cycle 1.5 %

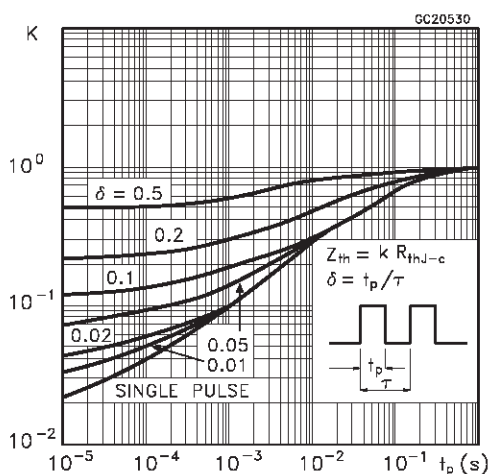
( $\bullet$ ) Pulse width limited by safe operating area

(1)  $I_{SD} \leq 60\text{ A}$ ,  $di/dt \leq 200\text{ A}/\mu\text{s}$ ,  $V_{DD} \leq V_{(BR)DSS}$ ,  $T_j \leq T_{JMAX}$

## Safe Operating Area

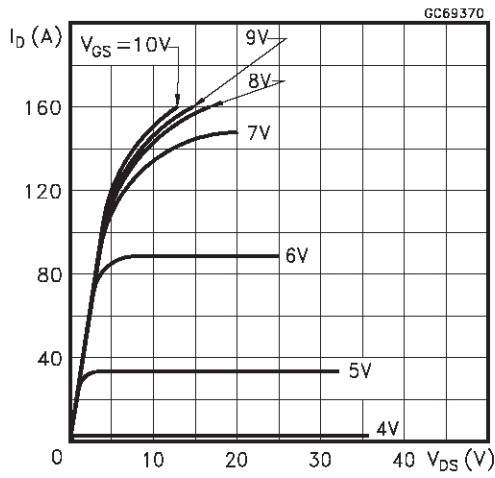


## Thermal Impedance

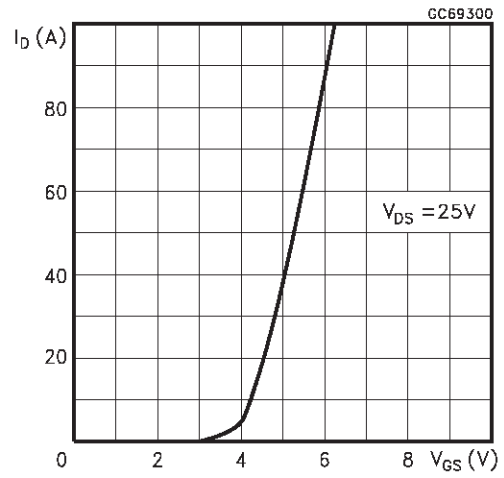


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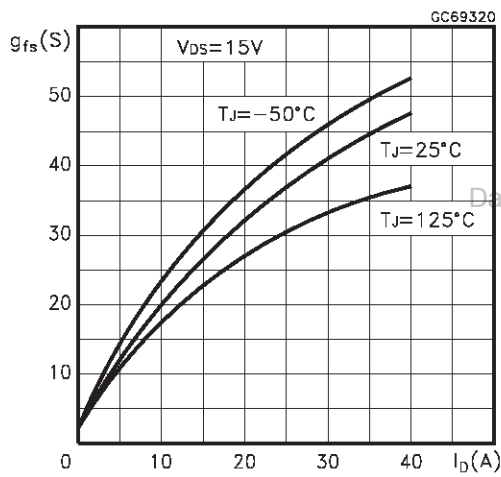
Output Characteristics



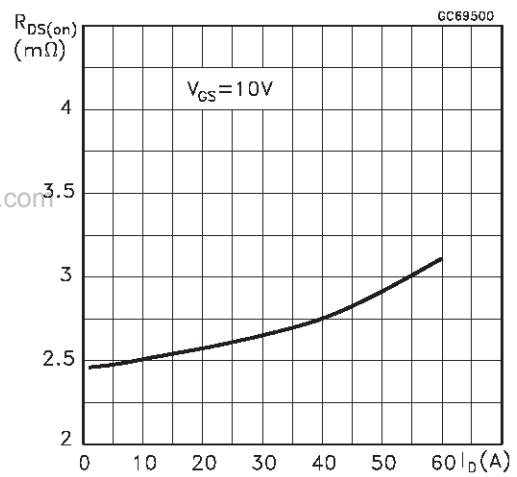
Transfer Characteristics



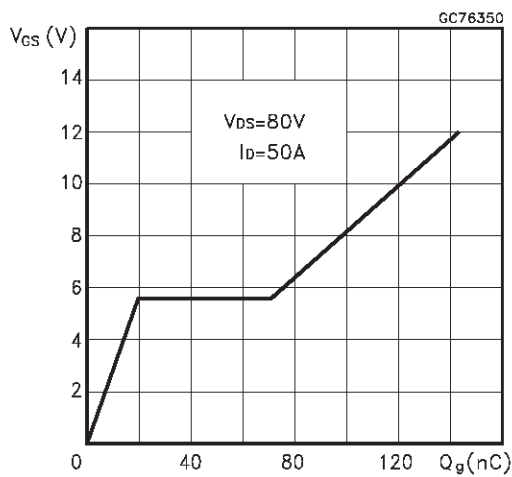
Transconductance



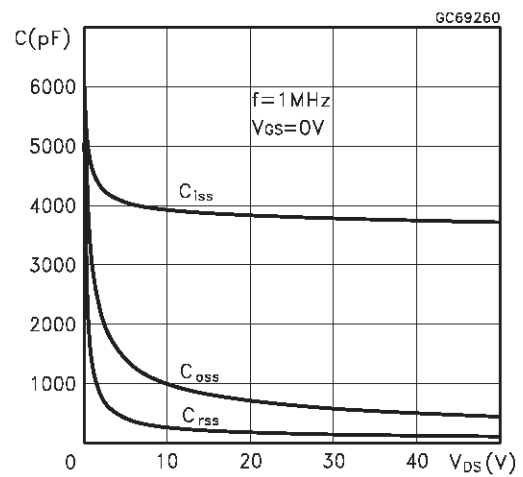
Static Drain-source On Resistance



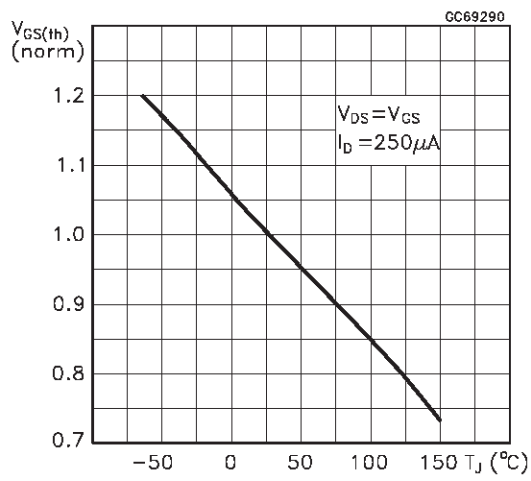
Gate Charge vs Gate-source Voltage



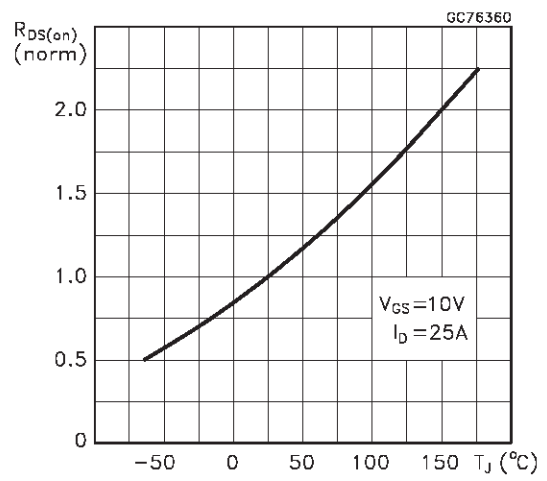
Capacitance Variations



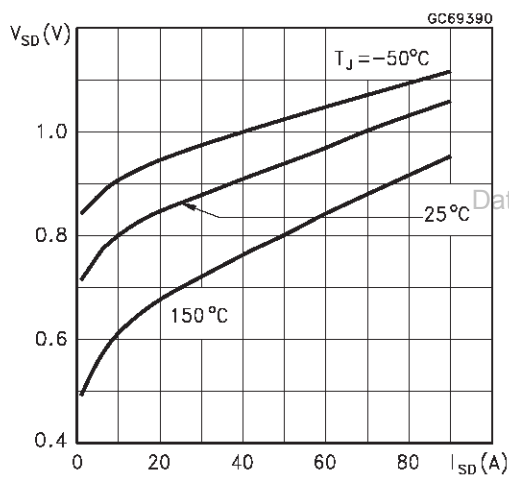
Normalized Gate Threshold Voltage vs Temperature



Normalized On Resistance vs Temperature

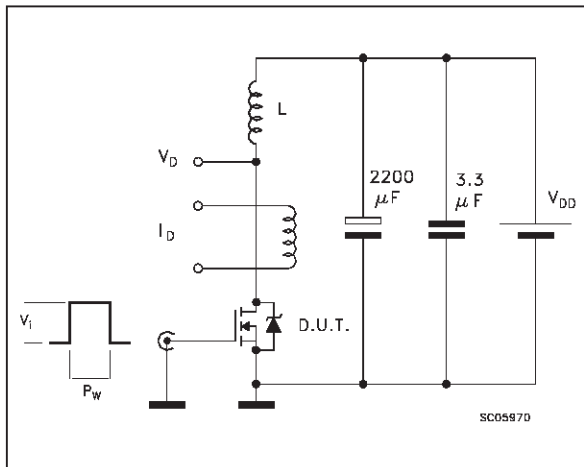


Source-drain Diode Forward Characteristics

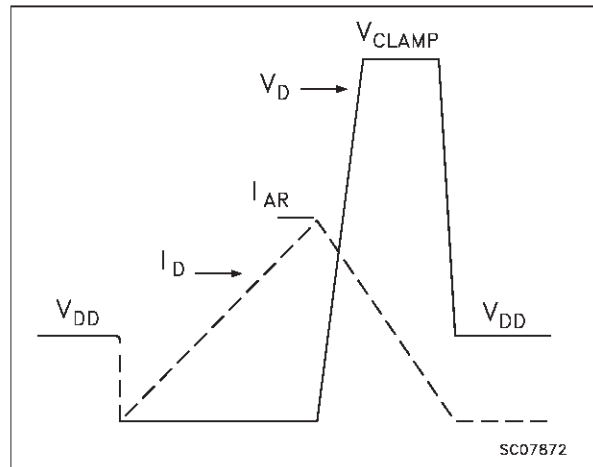


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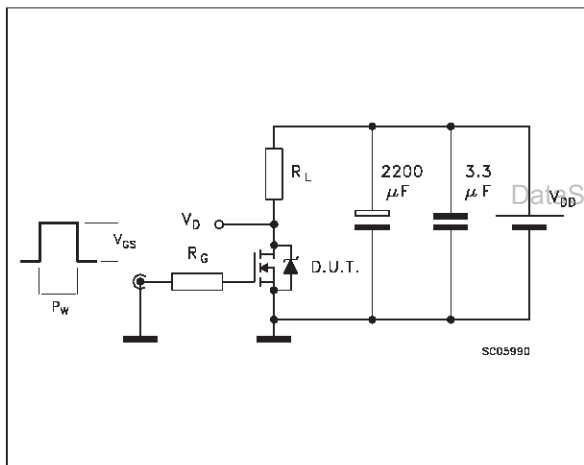
**Fig. 1: Unclamped Inductive Load Test Circuit**



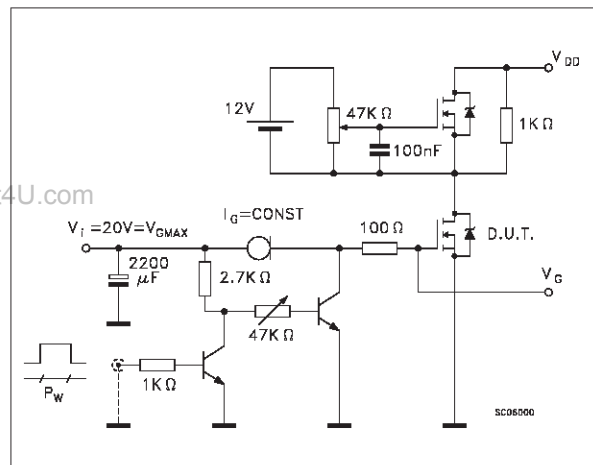
**Fig. 2: Unclamped Inductive Waveform**



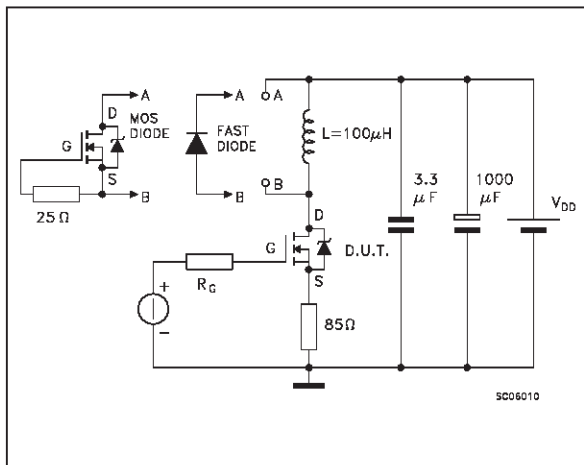
**Fig. 3: Switching Times Test Circuits For Resistive Load**



**Fig. 4: Gate Charge test Circuit**

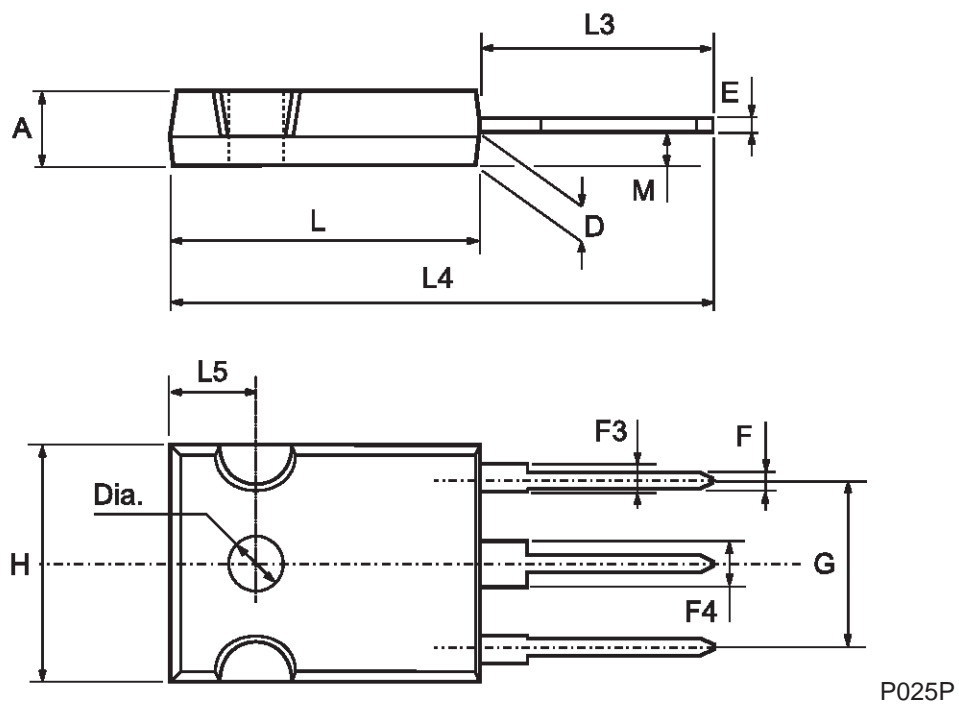


**Fig. 5: Test Circuit For Inductive Load Switching And Diode Recovery Times**



## TO-247 MECHANICAL DATA

DIM.	mm			inch		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
A	4.7		5.3	0.185		0.209
D	2.2		2.6	0.087		0.102
E	0.4		0.8	0.016		0.031
F	1		1.4	0.039		0.055
F3	2		2.4	0.079		0.094
F4	3		3.4	0.118		0.134
G		10.9			0.429	
H	15.3		15.9	0.602		0.626
L	19.7		20.3	0.776		0.779
L3	14.2		14.8	0.559	0.413	0.582
L4		34.6			1.362	
L5		5.5			0.217	
M	2		3	0.079		0.118
Dia	3.55		3.65	0.140		0.144



## STW50N10

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